

128Kx8 Static RAM CMOS, Module

The ED18F8128C* is a 1024K bit CMOS Static RAM based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered epoxy laminate (FR-4) substrate.

An on-board decoder circuit interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the ED18F8128C requires no clocks or refreshing for operation.

Features

128Kx8 bit CMOS Static
Random Access Memory

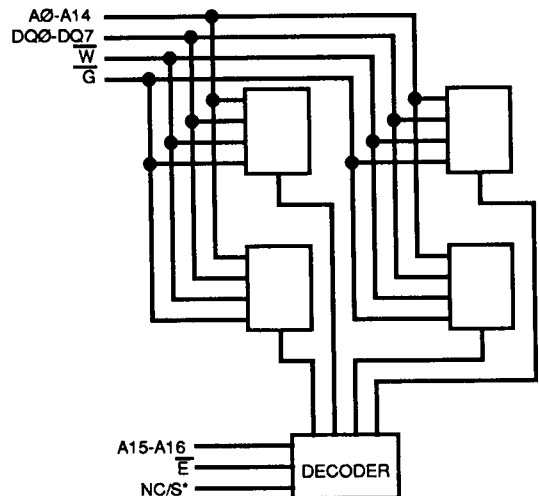
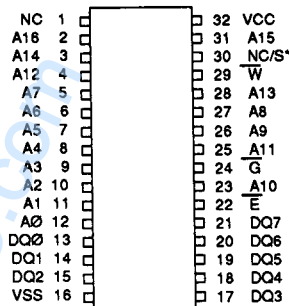
- Access Times 30 thru 150ns
- E, S*, and G Functions for Bus Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout

- 600 mil wide, 32 pin DIP Module, No. 112
- 400 mil wide, 32 pin DIP Module, No. 113

Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram



Pin Names

| | |
|----------------|--------------------------|
| A0-A16 | Address Inputs |
| E | Chip Enable |
| S* | Chip Select |
| \overline{W} | Write Enable |
| \overline{G} | Output Enable |
| DQ0-DQ7 | Common Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |
| NC | No Connection |

*ED18F8130C is identical to the ED18F8128C, with an additional chip select line (S). This additional chip select line can be used to provide system memory security during power down in non-battery backed up systems and to simplify decoding schemes in memory banking where large multiple pages of memory are required.

Absolute Maximum Ratings*

| | |
|--|-----------------|
| Voltage on any pin relative to VSS | -0.5V to 7.0V |
| Operating Temperature TA (Ambient) | |
| Commercial | 0°C to +70°C |
| Industrial | -40°C to +85°C |
| Storage Temperature | |
| Plastic | -55°C to +125°C |
| Power Dissipation | 1 Watt |
| Output Current | 20 mA |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-----|------|-----|-----|-------|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | - | 6.0 | V |
| Input Low Voltage | VIL | -0.3 | - | 0.8 | V |

AC Test Conditions

| | |
|--|------------------|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load 35-70ns | 1TTL, CL = 30pF |
| 100-150ns | 1TTL, CL = 100pF |
| (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF) | |

DC Electrical Characteristics

| Parameter | Sym | Conditions | Min | Typ* | Max | Units |
|------------------------------------|------|---|-----|------|----------|---------|
| Operating Power Supply Current | ICC1 | $\overline{W}, \overline{E} = VIL, I/O = 0mA, \text{Min Cycle}$ | -- | 70 | 220 | mA |
| Standby (TTL) Power Supply Current | ICC2 | $\overline{E} \geq VIH, VIN \leq VIL \text{ or } \geq VIH$ | -- | 10 | 130 | mA |
| Full Standby Power Supply Current | ICC3 | $\overline{E} \geq VCC-0.2V$ $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$ | -- | 1 | 20 | mA |
| Input Leakage Current | ILI | $VIN = 0V \text{ to } VCC$ | -- | -- | ± 10 | μA |
| Output Leakage Current | ILO | $V I/O = 0V \text{ to } VCC$ | -- | -- | ± 10 | μA |
| Output High Voltage | VOH | $IOH = -4.0mA$ | 2.4 | -- | -- | V |
| Output Low Voltage | VOL | $IOL = 8.0mA$ | -- | -- | 0.4 | V |

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

| \overline{G} | \overline{E} | \overline{W} | Mode | Output | Power |
|----------------|----------------|----------------|-----------------|--------|------------|
| X | H | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | Output Deselect | High Z | ICC1 |
| L | L | H | Read | DOUT | ICC1 |
| X | L | L | Write | DIN | ICC1 |

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|--|------|-----|------|
| Input Capacitance (Except DQ Pins) | CI | 25 | pF |
| Capacitance Control (DQ Pins) | CD/Q | 40 | pF |
| Input Capacitance Control Lines (\overline{E}) | CC | 30 | pF |
| Input Capacitance \overline{W} Line | CW | 30 | pF |

These parameters are sampled, not 100% tested.

AC Characteristics

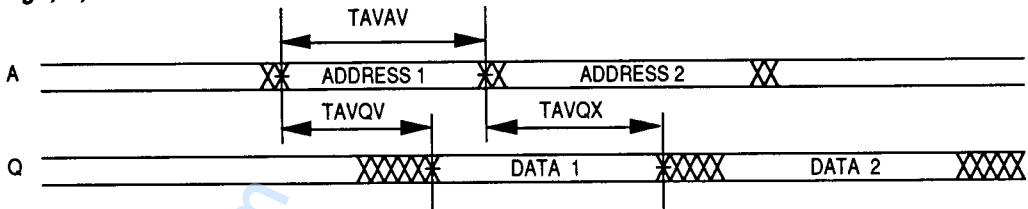
Read Cycle

| Parameter | Symbol | 30ns | | 35ns | | 45ns | | 55ns | | Units |
|--|--------|------|-----|------|-----|------|-----|------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 30 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | TAVQV | | 30 | | 35 | | 45 | | 55 | ns |
| Chip Enable Access Time | TELQV | | 30 | | 35 | | 45 | | 55 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | 5 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output Valid | TGLQV | | 20 | | 25 | | 35 | | 40 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 3 | | 3 | | 3 | | 3 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | | 20 | | 25 | | 35 | | 40 | ns |
| Output Disable to Output in High Z (1) | TGHQZ | | 15 | | 15 | | 20 | | 25 | ns |
| Output Hold from Address Change | TAVQX | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

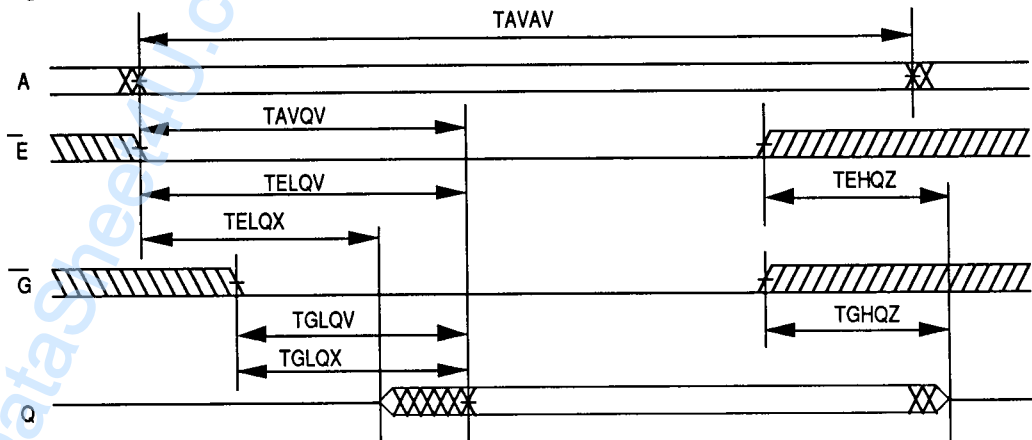
Read Cycle 1

W High; G, E Low



Read Cycle 2

W High



AC Characteristics

Read Cycle

| Parameter | Symbol | 70ns | | 100ns | | 120ns | | 150ns | | Units |
|---------------------------------------|--------|------|-----|-------|-----|-------|-----|-------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 70 | | 100 | | 120 | | 150 | | ns |
| Address Access Time | TAVQV | | 70 | | 100 | | 120 | | 150 | ns |
| Chip Enable Access Time | TELQV | | 70 | | 100 | | 120 | | 150 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | 5 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output Valid | TGLQV | | 50 | | 50 | | 60 | | 70 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 10 | | 10 | | 5 | | 5 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | | 30 | | 30 | | 40 | | 50 | ns |
| Output Disable to Output in High Z(1) | TGHQZ | | 30 | | 30 | | 40 | | 50 | ns |
| Output Hold from Address Change | TAVQX | 10 | | 10 | | 10 | | 10 | | ns |

Note 1: Parameter guaranteed, but not tested.

AC Characteristics

Write Cycle

| Parameter | Symbol | | 30ns | | 35ns | | 45ns | | 55ns | | Units |
|--|--------|----------------|------|-----|------|-----|------|-----|------|-----|-------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 30 | | 35 | | 45 | | 55 | | ns |
| Chip Enable to End of Write | TELWH | \overline{W} | 25 | | 30 | | 40 | | 50 | | ns |
| | TWLEH | \overline{E} | 20 | | 25 | | 30 | | 35 | | ns |
| Address Setup Time | TAVWL | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVEL | \overline{E} | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to End of Write | TAVWH | \overline{W} | 25 | | 30 | | 40 | | 50 | | ns |
| | TAVEH | \overline{E} | 25 | | 30 | | 40 | | 50 | | ns |
| Write Pulse Width | TWLWH | \overline{W} | 20 | | 25 | | 30 | | 35 | | ns |
| | TELEH | \overline{E} | 25 | | 30 | | 40 | | 50 | | ns |
| Write Recovery Time | TWHAX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| Data Hold Time | TWHDX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHDX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| Write to Output in High Z (1) | TWLQZ | | | 12 | | 15 | | 20 | | 25 | ns |
| Data to Write Time | TDVWH | \overline{W} | 15 | | 20 | | 20 | | 25 | | ns |
| | TDVEH | \overline{E} | 15 | | 20 | | 20 | | 25 | | ns |
| Output Active from End of Write (1) | TWHQX | | 0 | | 0 | | 0 | | 0 | | ns |

Note 1: Parameter guaranteed, but not tested.

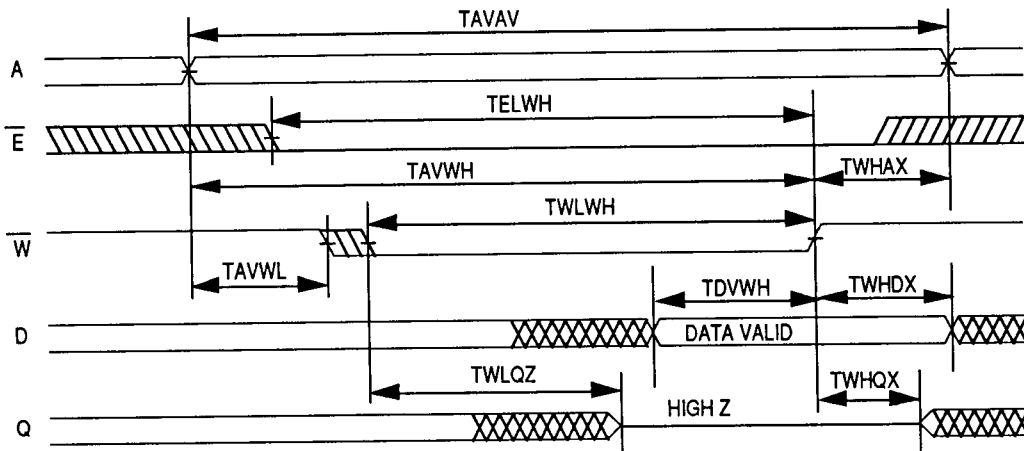
AC Characteristics

Write Cycle

| Parameter | Symbol | | 70ns | | 100ns | | 120ns | | 150ns | | Units |
|--|--------|----------------|------|-----|-------|-----|-------|-----|-------|-----|-------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 70 | | 100 | | 120 | | 150 | | ns |
| Chip Enable to | TELWH | \overline{W} | 55 | | 80 | | 85 | | 70 | | ns |
| End of Write | TWLEH | \overline{E} | 55 | | 80 | | 85 | | 70 | | ns |
| Address Setup Time | TAVWL | \overline{W} | 20 | | 20 | | 20 | | 20 | | ns |
| | TAVEL | \overline{E} | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | \overline{W} | 55 | | 80 | | 90 | | 110 | | ns |
| End of Write | TAVEH | \overline{E} | 60 | | 80 | | 85 | | 90 | | ns |
| Write Pulse Width | TWLWH | \overline{W} | 60 | | 70 | | 70 | | 80 | | ns |
| | TELEH | \overline{E} | 55 | | 80 | | 90 | | 110 | | ns |
| Write Recovery Time | TWHAX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| Data Hold Time | TWHDX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHDX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| Write to Output in High Z (1) | TWLQZ | | 0 | 35 | 0 | 35 | 0 | 35 | 0 | 45 | ns |
| Data to Write Time | TDVWH | \overline{W} | 25 | | 35 | | 40 | | 50 | | ns |
| | TDVEH | \overline{E} | 25 | | 35 | | 40 | | 50 | | ns |
| Output Active from End of Write (1) | TWHQX | | 0 | | 0 | | 0 | | 0 | | ns |

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W Controlled



Write Cycle 2
E Controlled

